REMARKS

Claims 21-27, 29 and 32-34 are pending in the application.

Claims 21-27, 29 and 32-34 have been rejected.

Claims 1, 3, 5-7, 28, and 30-31 are withdrawn from consideration, and canceled without prejudice.

Claims 21-25, 27, 29, 32, and 33 have been amended as set forth herein. The amendments to Claims 21-25, 27, 29, 32, and 33 are strictly for formality and are not related to issues of patentability.

New Claims 35-47 have been added. The support for the new claims can be found, for example, in Paragraphs [0018] to [0027] of the Applicant's published application. The Applicant respectfully submits that no new subject matter is being added and respectfully requests entry of new Claims 35-47.

Reconsideration of the claims is respectfully requested.

I. CLAIM REJECTIONS -- 35 U.S.C. § 103

Claims 21, 25, 26, 32 and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,423,076 to *Westergren* (hereinafter "Westergren") in view of U.S. Patent No. 5,319,798 to *Watanabe* (hereinafter "Watanabe"). The Applicant respectfully traverses the rejection.

Claims 22-24, 27, 29 and 33 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Westergren in view of Watanabe, and further in view of U.S. Patent 5,794,131 to *Cairns* (hereinafter, "Cairns"). The Applicant respectfully traverses the rejection.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a prima facie case of obviousness. MPEP § 2142, p. 2100-133 (8th ed. rev. 4, October 2005). Absent such a prima facie case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.* To establish a *prima facie* case of obviousness, three basic criteria must be met: *Id.* First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *Id.* Second, there must be a reasonable expectation of success. *Id.*

Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *Id.* The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *Id.*

The Applicant respectfully submits that the combination of cited references fails to teach or suggest all the claim elements of independent Claim 21. Specifically, Claim 21 recites "wherein when the transceiver is in a receiving mode, the digital synthesizer is configured to receive a non-modulation signal, generate a non-modulated reference signal, and transmit the non-modulated reference signal to the phase locked loop."

The Office Action appears to suggest that Watanabe discloses this element of Claim 21. For ease of reference, those sections of Watanabe cited in the Office Action are set forth below:

> Therefore, an object of the present invention is to provide a transceiver of such a TDMA communications system which requires a frequent switching of a transmitting signal and receiving signal and whose transmitting and receiving portions share a single PLL frequency synthesizer as their local frequency signal sources, and in which any unlock alarm is not produced for a predetermined time period immediately after a frequency switching even if there is an unlock condition of the PLL frequency synthesizer within the time period. (Col. 1, lines 58-67.)

The Applicant is unable to find any teaching or suggestion of (1) a non-modulation signal and (2) a non-modulated reference signal in this section or any section of Watanabe. The Office Action further cites the following section of Watanabe:

> The PLL synthesizer 5 comprises a PLL composed of a voltage-controlled oscillator 51 responsive to a control voltage S31 to supply a local oscillating signal S36 having a predetermined frequency to a synthesizer output terminal 501. A variable frequency divider 55 frequency-divides the signal S36 to produce a comparative signal S34 under control of a dividing data signal S37 supplied from a dividing data input terminal 502 for instructing a dividing ratio and as to the strobe signal supplied from a strobe signal input terminal 503 for activating the dividing data signal S37. A reference oscillator 54 supplies a reference signal S33 having a reference frequency to a phase detector 53 which compares in phase, the comparative signal S34 with the reference signal S33 to produce a phase difference signal S32. A low pass filter 52 integrates the phase difference signal S32 to produce the above-mentioned control voltage S31. The local oscillating signal S13 supplied from the PLL synthesizer 5 in

> FIG. 1 corresponds to the frequency signal S36 and the frequency control signal S16a for controlling the frequency of the local oscillating signal S13 is divided into the dividing data signal S37 and the strobe signal S38. (Col. 5, lines 37-59.)

Again, the Applicant is unable to find any teaching or suggestion of (1) a non-modulation signal and (2) a non-modulated reference signal in this section or any section of Watanabe. If such a teaching can be found, the Applicant respectfully requests that the Office Action specifically point out these two elements in Watanabe.

In distinct contrast, Paragraph [0026] of the Applicant's published application states:

> [0026] Then, mode detector 41 detects the transceiver, during a second time-interval, being in a receiving mode, for example via a coupling not shown to receiver part 4, and/or for example by making a calculation, with said first and second time slots being standardized, and informs processor/memory system 42, which possibly instructs non-modulation signal generator 44 to generate a non-modulation signal (for example a dc-voltage adaptable via processor/memory system 42 or a ground voltage in which case said instructing does not necessarily have to take place) and instructs control signal generator 43 to generate a second control signal. In response to this second control signal, switch 32 supplies said non-modulation signal originating from non-modulation signal generator 44 to DDS 24, and switch 11 couples second filter 13 to VCO 10, with second filter 13 for example being a narrow band filter allowing demodulation with reduced phase noise. DDS 24 now generates a non-modulated reference signal (due to said non-modulation signal now not manipulating said control words but either supplying/defining predefined/fixed control words or not supplying/defining any control words at all in which case DDS 24 will use its own predefined/fixed values), which is supplied to PLL 10-15, which, via phase detector 14 and second filter 12 and switch 11 and VCO 10, with divider 15 being in a feedback loop, locks this non-modulated reference signal. The locked non-modulated reference signal is supplied via switch 5 to demodulator 6, due to switch 5, for example in response to said second control signal or a further control signal originating from controller 40, connecting VCO 10 with demodulator 6. Receiver part 4, for example comprising a filter, a low noise amplifier and an auto gain controller, receives a (modulated) radio signal via antenna I and switch 3. Switch 3, for example in response to said second control signal or a further control signal originating from controller 40 via a coupling not shown, connects antenna 1 with receiver part 4, and supplies a gain controlled, amplified and filtered (modulated) radio signal to demodulator 6, which demodulates (for example via a Zero IF mode or Near Zero IF mode, which is very advantageous in that no expensive and bulky SAW IF filters are required) said last mentioned signal via said locked non-modulated reference signal. As a result, a demodulated signal is supplied to

> controller 40, for example via processor/memory system 42 to a man-machine-interface not shown which in response generates an audio signal. So, during this second time-interval, the transceiver is in a receiving mode, and the DDS driven PLL 24,10-15 is in an oscillating state.

Independent Claims 25, 32, and 34 also recite limitations analogous to the novel limitations emphasized above in traversing the rejection of Claim 21 and, therefore, also are patentable over the combination of cited references.

With respect to the rejection of dependent Claims 22-24, 27, 29 and 33 over Westergren, Watanabe, and Cairns, for the same or similar reasons set forth above, and because the cited portions of Westergren and Cairns fail to cure the noted deficiency in Watanabe, these claims are also patentable.

Accordingly, the Applicant respectfully requests withdrawal the § 103 rejections with respect to these claims.

II. NEW CLAIMS

New Claims 35-47 have been added. At a minimum, the Applicant respectfully submits that Claims 35-47 are patentable for the reasons discussed above. The Applicant respectfully requests entry and full allowance of Claims 35-47.

III. CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *rmccutcheon@munckcarter.com.*

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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